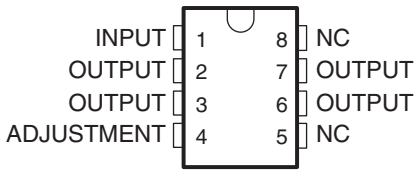
FEATURES

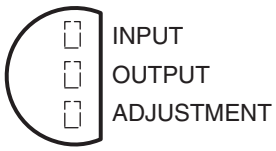
- **Output Voltage Range Adjustable 1.2 V to 32 V When Used With External Resistor Divider**
- **Output Current Capability of 100 mA**
- **Input Regulation Typically 0.01% Per Input-Voltage Change**
- **Output Regulation Typically 0.5%**
- **Ripple Rejection Typically 80 dB**
- **For Higher Output Current Requirements, See LM317M (500 mA) and LM317 (1.5 A)**

D OR PW PACKAGE
(TOP VIEW)

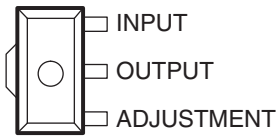


NC – No internal connection
OUTPUT terminals are all internally connected.

LP PACKAGE
(TOP VIEW)



PK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LM317L is an adjustable three-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.2 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

In addition to higher performance than fixed regulators, this regulator offers full overload protection, available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

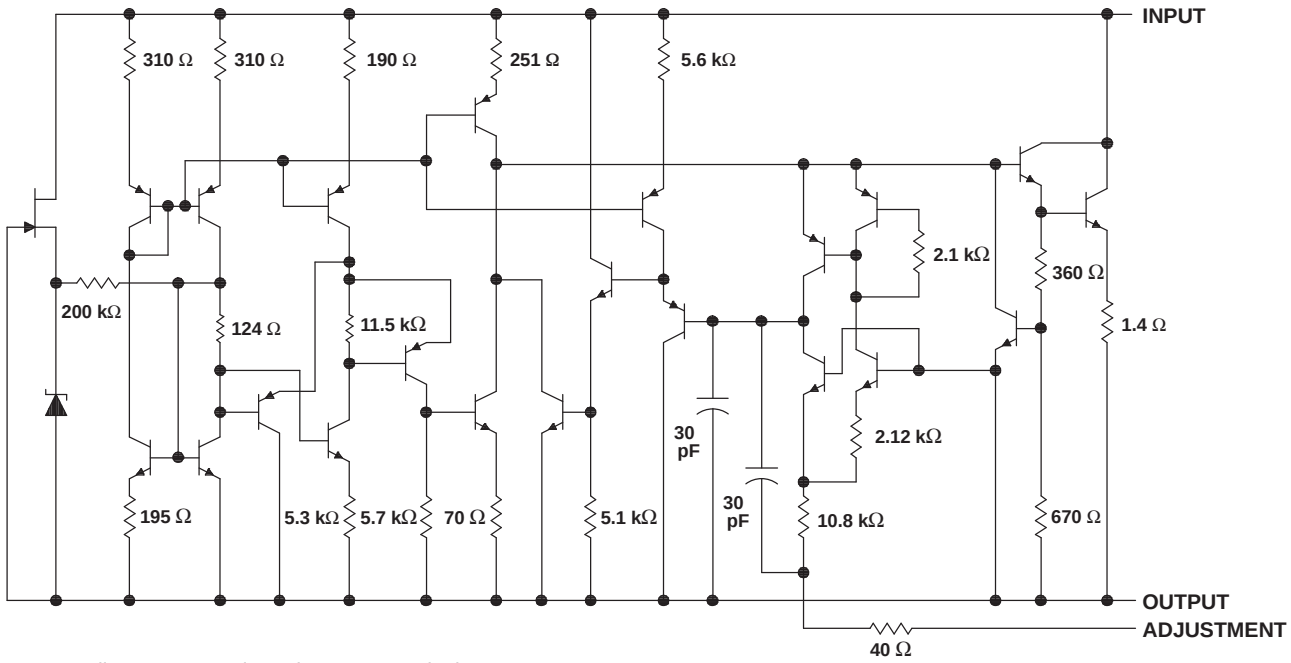
In addition to replacing fixed regulators, the LM317L regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.2 V, where most loads draw little current.

The LM317LC is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The LM317LI is characterized for operation over the virtual junction temperature range of –40°C to 125°C.

ORDERING INFORMATION

T_J	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	SOIC – D	Tube of 75	LM317LCD	L317LC
		Reel of 2500	LM317LCDR	
	SOT-89 – PK	Reel of 1000	LM317LCPK	LA
	TO-226/TO-92 – LP	Bulk of 1000	LM317LCLP	L317LC
		Reel of 2000	LM317LCLPR	
	TSSOP – PW	Tube of 150	LM317LCPW	L317LC
		Reel of 2000	LM317LCPWR	
–40°C to 125°C	SOIC – D	Tube of 75	LM317LID	L317LI
		Reel of 2500	LM317LIDR	
	SOT-89 – PK	Reel of 1000	LM317LIPK	LB
	TO-226/TO-92 – LP	Bulk of 1000	LM317LILP	L317LI
		Reel of 2000	LM317LILPR	
	TSSOP – PW	Tube of 150	LM317LIPW	L317LI
		Reel of 2000	LM317LIPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



NOTE A: All component values shown are nominal.

Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage			35	V
θ_{JA}	Package thermal impedance(2)	D package(3)		97.1	°C/W
		LP package(3)		139.5	
		PK package(4)		51.5	
		PW package(3)		149.4	
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions

			MIN	MAX	UNIT
$V_I - V_O$	Input-to-output voltage differential			35	V
I_O	Output current		2.5	100	mA
T_J	Operating virtual-junction temperature	LM317LC	0	125	°C
		LM317LI	–40	125	

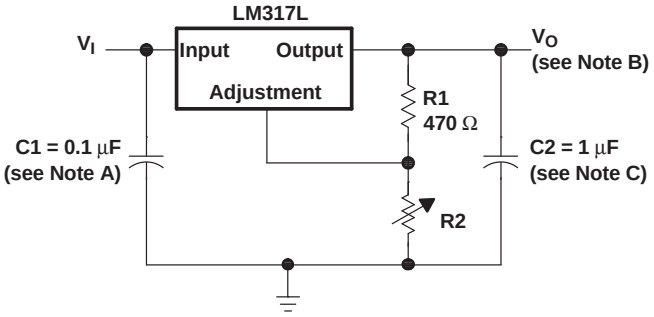
Electrical Characteristics

over recommended operating virtual-junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
Input voltage regulation(2)	$V_I - V_O$ = 5 V to 35 V	T_J = 25°C		0.01	0.02	%V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-µF capacitor between ADJUSTMENT and ground		66	80		
Output voltage regulation	V_I = 5 V to 35 V, T_J = 25°C, I_O = 2.5 mA to 100 mA,	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		50		mV
		$V_O \ge 5$ V		10		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C			10		mV/V
Output voltage long-term drift	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35 V			3	10	mV/V
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		30		µV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35$ V		100	200		mA
ADJUSTMENT current				50	100	µA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	µA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

(1) Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-µF capacitor across the input and a 1-µF capacitor across the output.
(2) Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

APPLICATION INFORMATION



NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from the filter capacitors.

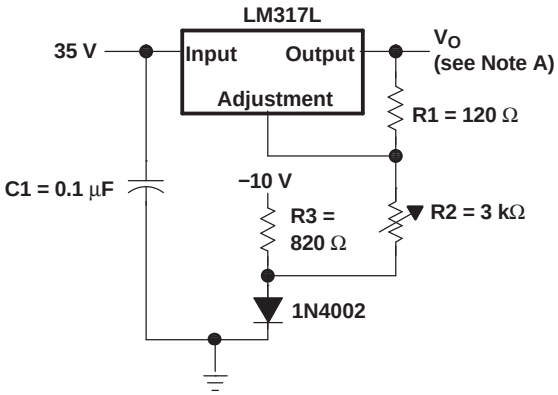
B. Output voltage is calculated from the equation:

$$V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈1.25 V).

C. Use of an output capacitor improves transient response, but is optional.

Figure 1. Adjustable Voltage Regulator

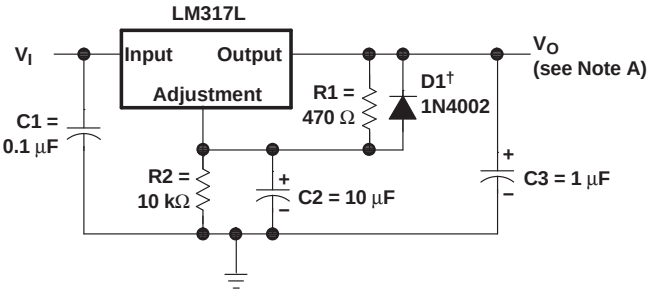


NOTE A: Output voltage is calculated from the equation:

$$V_O = V_{ref}\left(1 + \frac{R2 + R3}{R1}\right) - 10\ V$$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈1.25 V).

Figure 2. 0-V to 30-V Regulator Circuit



† D1 discharges C2 if output is shorted to ground.

NOTE A: Use of an output capacitor improves transient response, but is optional.

Figure 3. Regulator Circuit With Improved Ripple Rejection

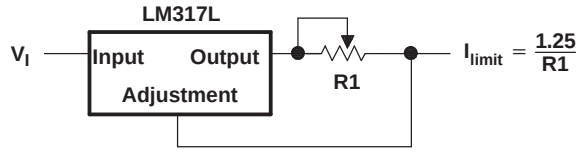


Figure 4. Precision Current-Limiter Circuit

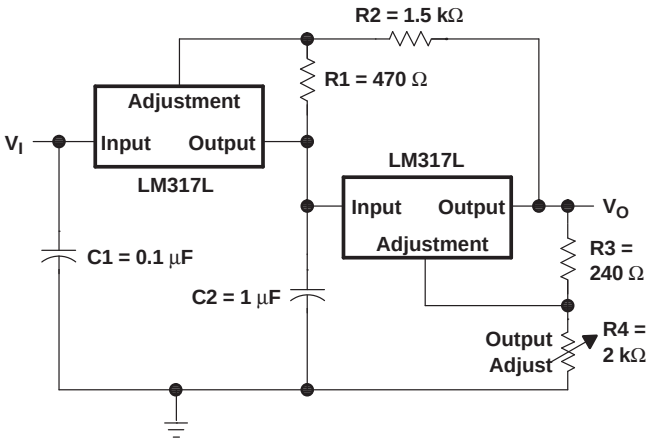


Figure 5. Tracking Preregulator Circuit

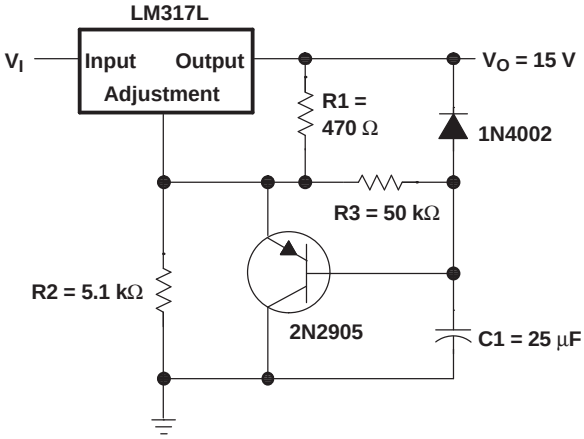


Figure 6. Slow-Turnon 15-V Regulator Circuit

APPLICATION INFORMATION (continued)

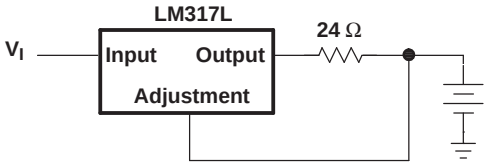


Figure 7. 50-mA Constant-Current Battery-Charger Circuit

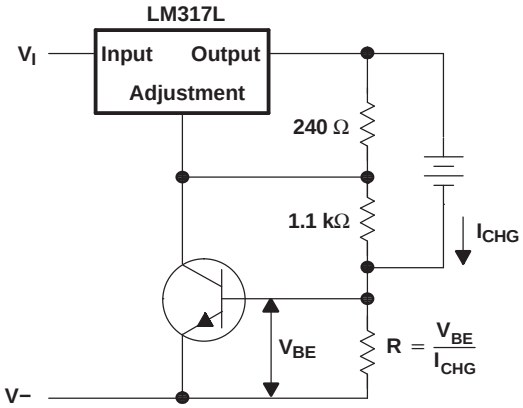
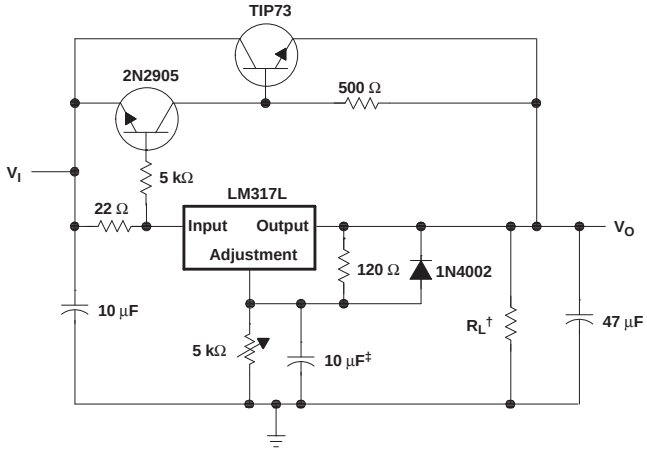


Figure 8. Current-Limited 6-V Charger



† Minimum load current is 30 mA.
‡ Optional capacitor improves ripple rejection.

Figure 9. High-Current Adjustable Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LM317LCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LCLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LCLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LCLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LCPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
LM317LCPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
LM317LCPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LCPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
LM317LILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317LIPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
LM317LIPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
LM317LIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM317LIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

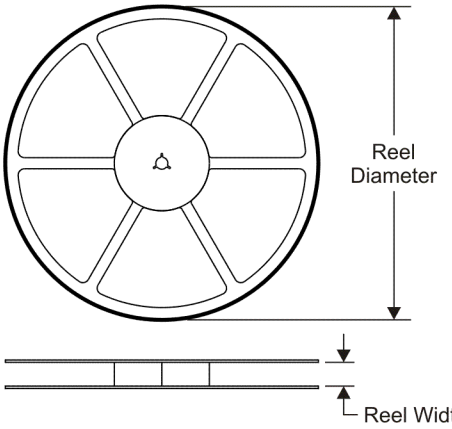
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

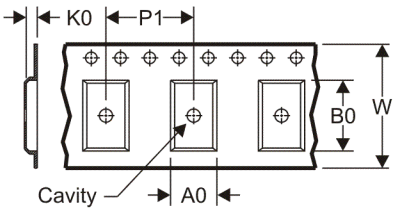
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

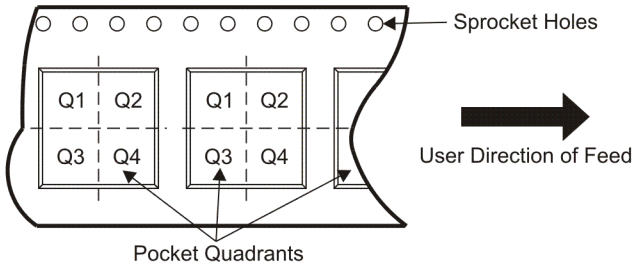


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

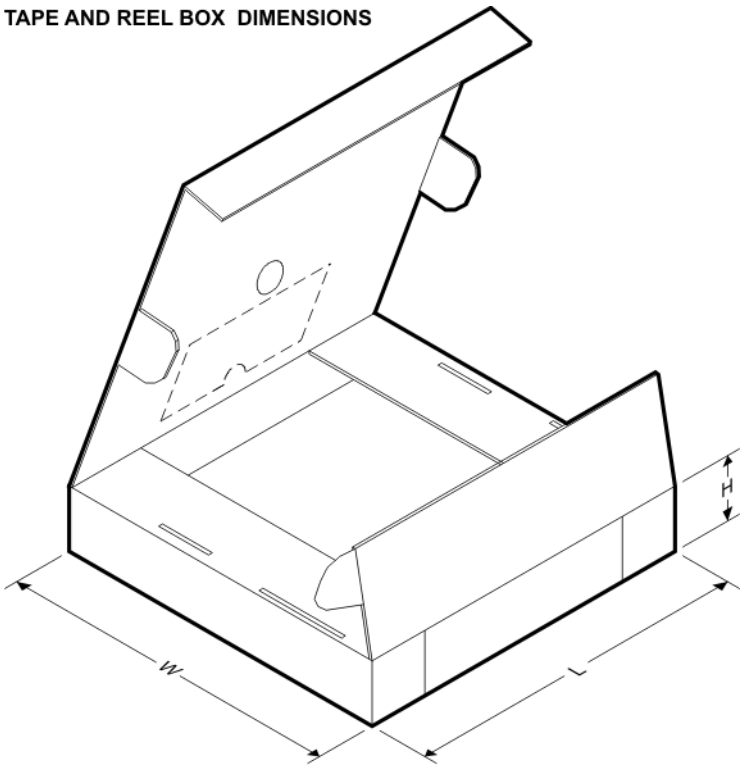
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317LCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM317LIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

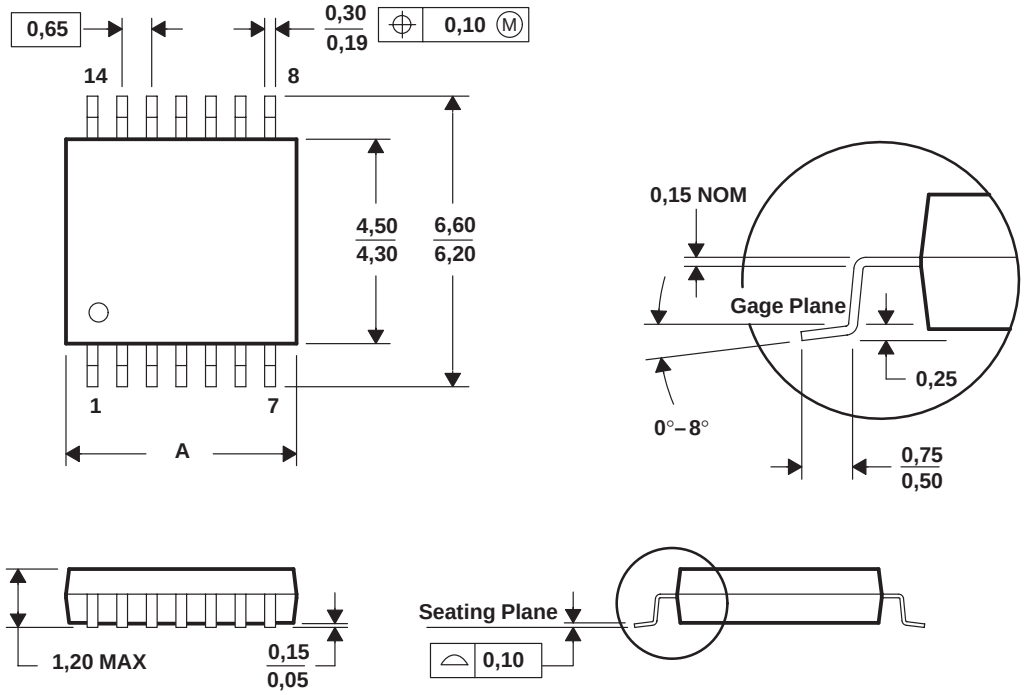


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM317LCDR	SOIC	D	8	2500	340.5	338.1	20.6
LM317LCPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
LM317LIDR	SOIC	D	8	2500	340.5	338.1	20.6
LM317LIPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

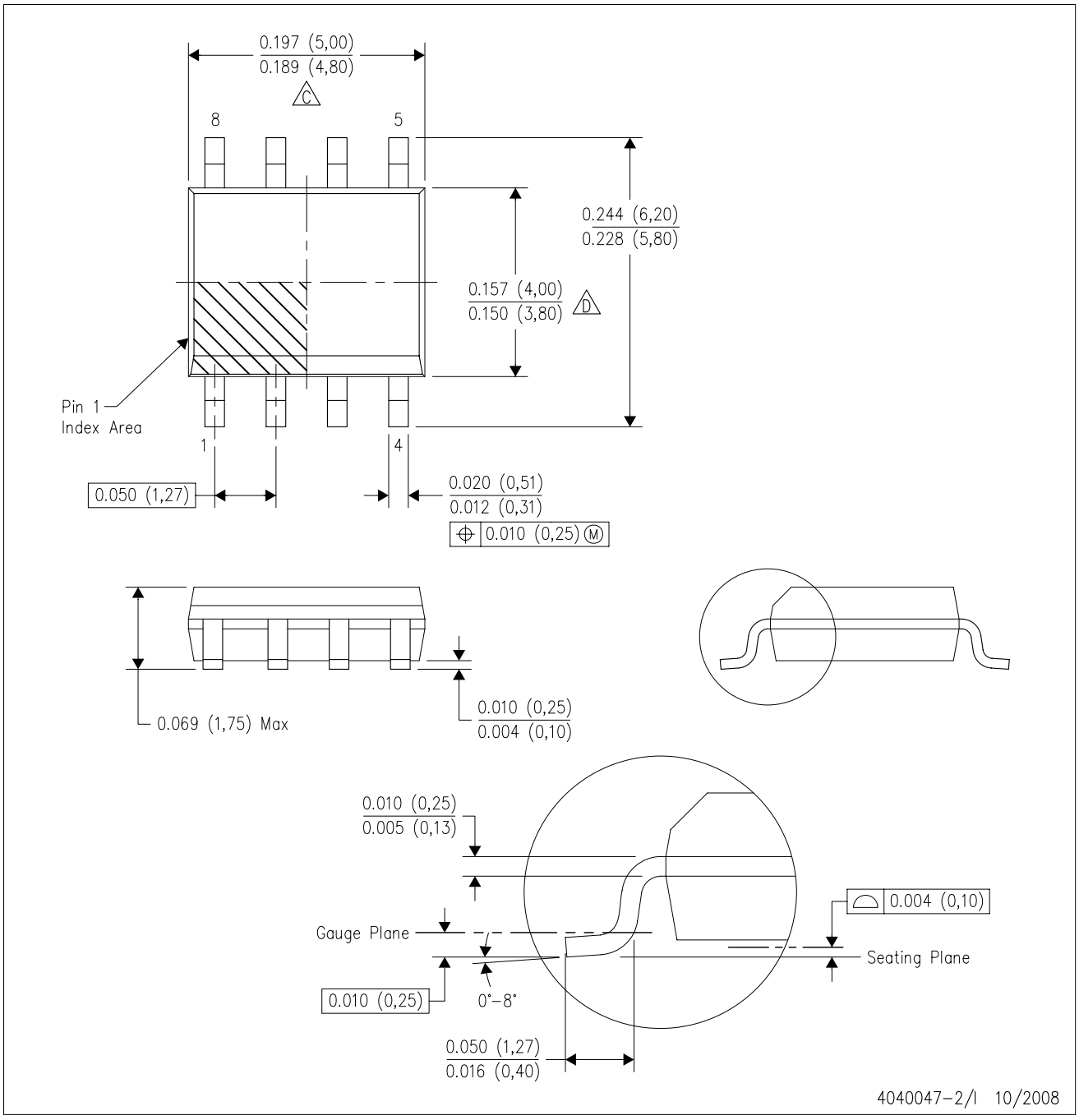


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

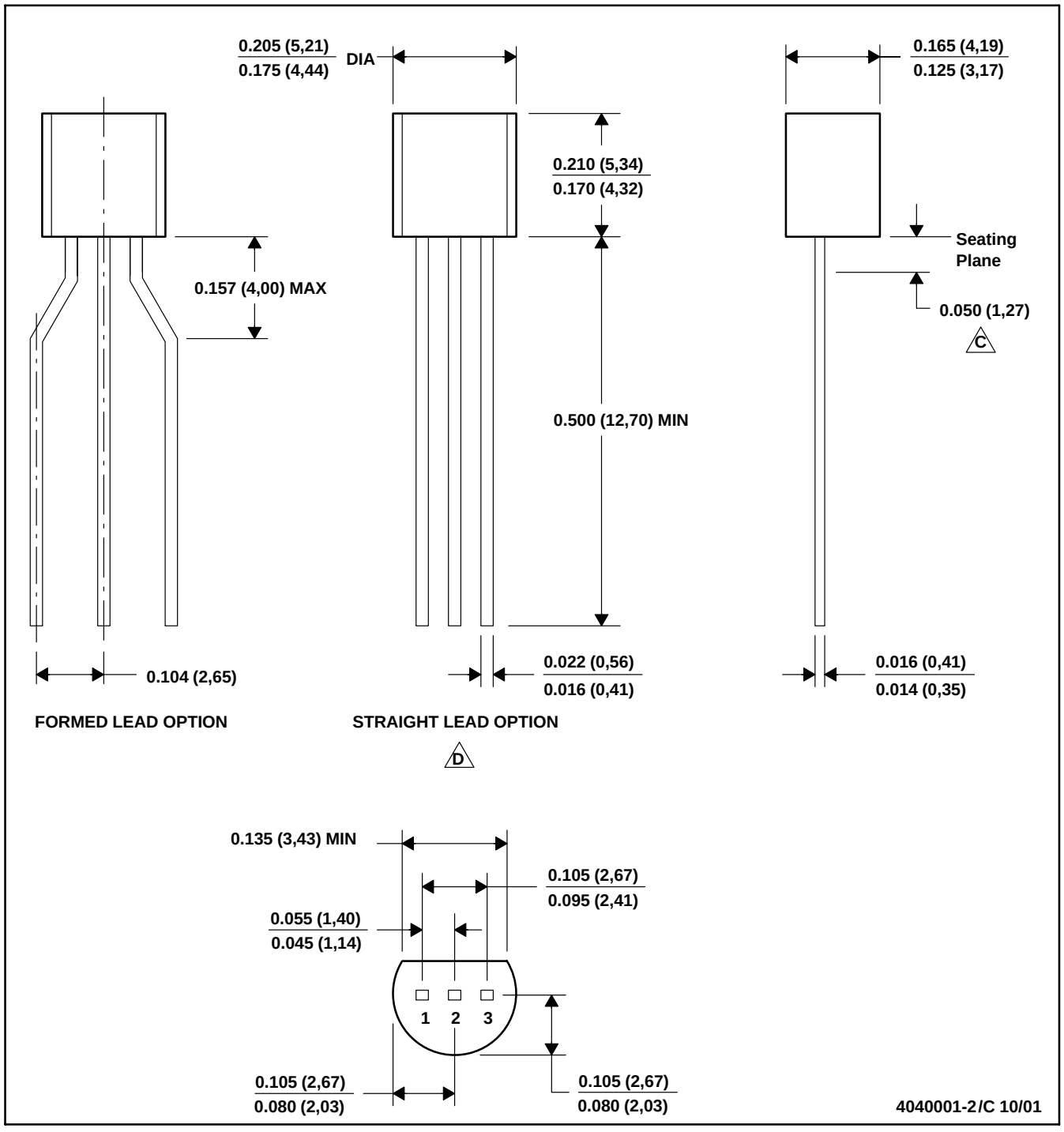
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



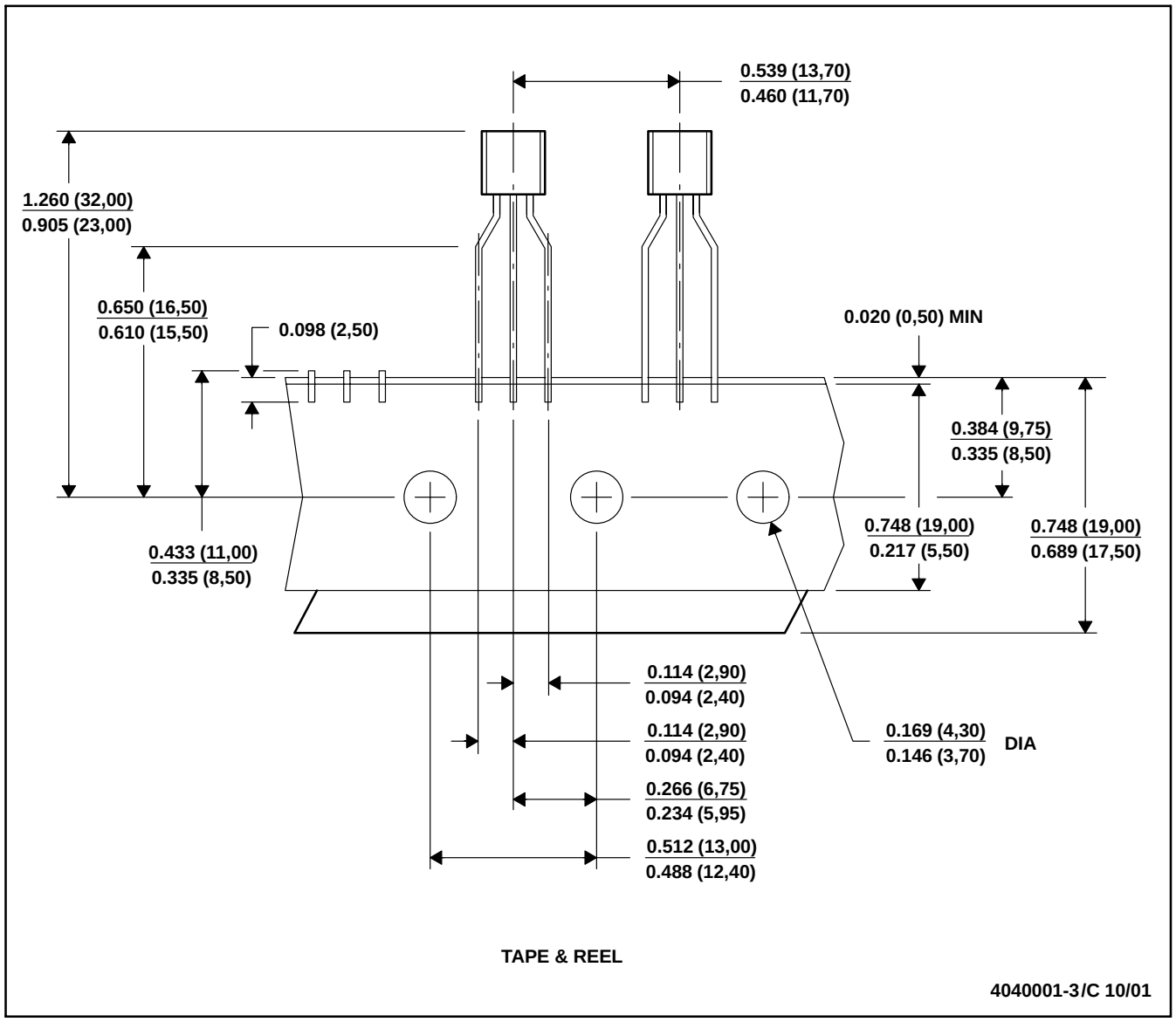
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**



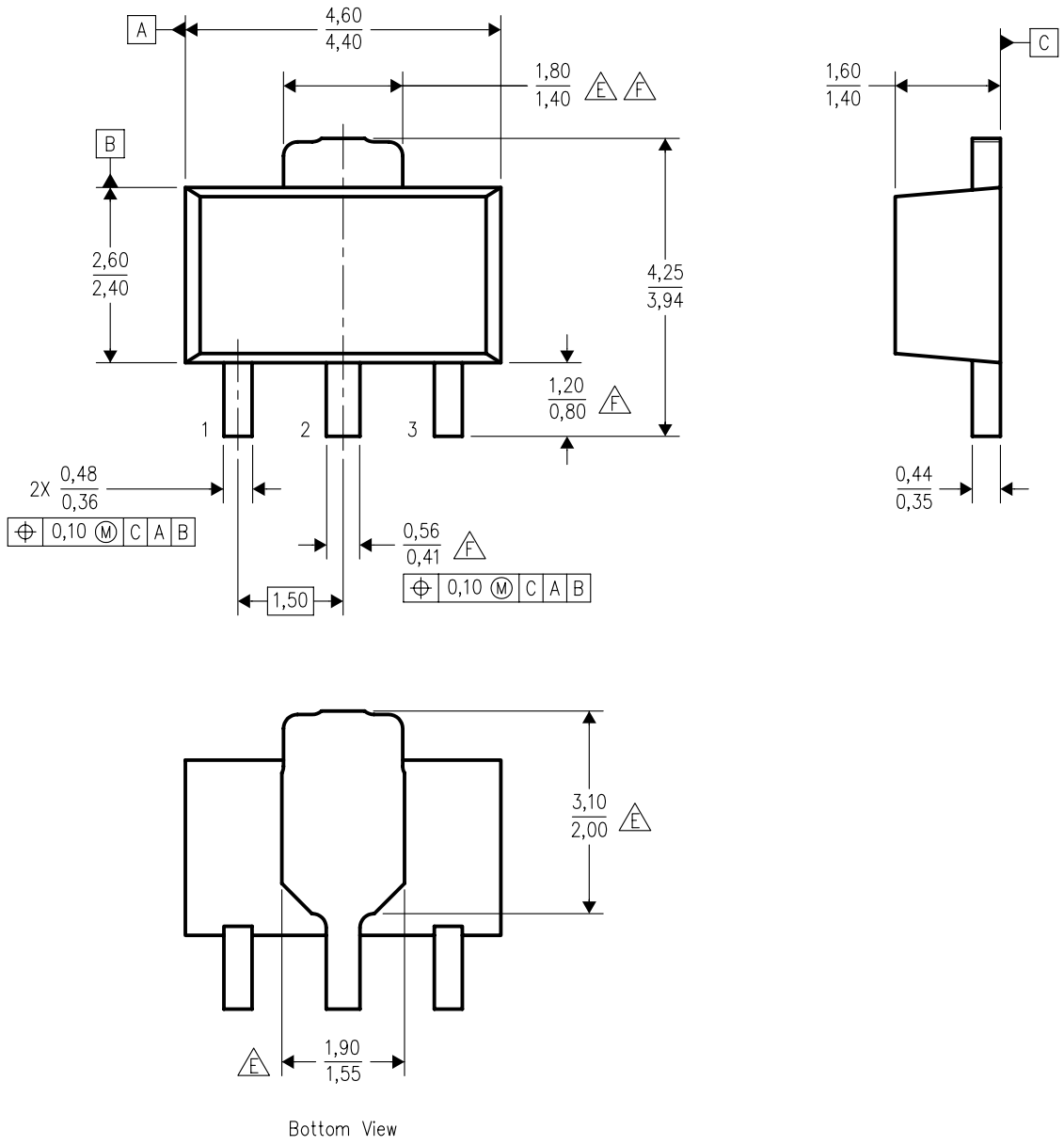
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area
D. FAlls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)
E. Shipping Method:
Straight lead option available in bulk pack only.
Formed lead option available in tape & reel or ammo pack.

LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Format Lead Option package.

PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

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